Power Optimization of GaAs Implanted FET's Based on Large-Signal Modeling

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Abstract—**Large-signal models for ion-implanted, MMIC-compatible GaAs FET's are reported using different techniques. There are (i) S-parameter measurements, (ii) low-frequency capacitances combined with dc $I-V$ characteristics, and (iii) physical data. The results obtained with each model are compared to high-frequency power measurements, and the relative merits of each technique are discussed. The models permit investigation of the influence of frequency, implantation energy, doping density, drain bias, recess depth, and gate length on the small- and large-signal FET parameters and saturation mechanisms. FET's fabricated with these data give optimum gain and power characteristics at the desired frequency of operation.**

I. Introduction

LARGE-SIGNAL FET models are important for technology optimization of power devices as well as for computer-aided design of monolithic microwave integrated circuits (MMIC's), where highly accurate modeling is necessary. Technology optimization requires the development of specific models based on device physical parameters.

Many attempts have been made to find models to predict FET power characteritics at different frequencies, biasing, and load conditions [2]–[4], [19]–[21].

Large-signal models can be classified according to their input data (Fig. 1) as models using low-frequency measurements [3], [4], [19], [21], models based on high-frequency S-parameter measurements [2], [24], or models using device physical parameters and geometry [20].

To investigate the relative merits of each technique, we present here large-signal models of each of the above types (Sections II–IV). These were applied to ion-implanted GaAs FET's made with the same MMIC-compatible technology. A systematic comparion of the obtained results is presented in Section V, together with measurement verifications. Since our models can be used to predict not only FET saturation characteristics, but also large-signal device parameters, the results given in this paper can be used to better understand FET power operation and saturation mechanisms. Large-signal device parameters have been examined with respect to their dependence on frequency (Section VI), implantation energy (Section VII), carrier density and drain bias (Section VIII), recess (Section IX), and gate length (Section X).

The large-signal models presented in this paper are limited to the fundamental frequency of operation of FET's. Particular limitations for each model are mentioned in the appropriate sections.

II. The Use of Small-Signal Microwave Characteristics for Evaluation of FET Large-Signal Behavior: High-Frequency Model (HFM)

The FET small-signal, high-frequency characteristics can be evaluated by S-parameter measurements. Optimization techniques can be used to fit the element values of its equivalent circuit to the S-matrix. The accuracy of these models depends on the measurement precision and de-embedding accuracy, as well as on the mathematical method used for element optimization. Network calibration standards of configuration similar to the characterized devices (1 mm × 1 mm × 0.1 mm chips with 50-Ω gate and drain line terminals) can be used to reduce the measurement error to ±1° and ±0.1 dB over 2–18-GHz bandwidths [1]. De-embedding errors can be minimized by applying a self-calibration procedure at the chip level, using through, delay, and open-line standards. By employing such techniques, a maximum error of 1 percent was obtained between measured and modeled S-parameters, while typical measurement reproducibilities were of the order of 0.1 percent. The FET model is shown in Fig. 2. G_{gf} is the conductance of the forward-biased gate source junction, and G_{dg} models avalanche current. G_{gf} and G_{dg} are particularly important for large-signal FET operation. The bias dependence of device parameters was evaluated by 2–18-GHz S-parameter measurements at different gate V_{gso} and drain V_{dso} bias voltages. Mathematical expressions were evaluated for the dependence of such model parameters as C_{gs}, R_{ds}, and g_m on bias voltage, V_{gso}, and V_{dgo}. This was done by curve fitting, as explained in Appendix I. Fig. 3 gives such characteristics for the channel resistance $R_{ds}=1/G_{ds}$ of a 300-μm × 1-μm MESFET. The device was made by Si^{29} ion implantation ($E=280$ keV, $D=4\times10^{12}/cm^2$) into undoped semi-insulating (SI) substrates. The devices had an N^+ layer ($E=60$ keV, $D=2\times10^{13}/cm^2$) for reduction of access resistances and was recessed by 1900 Å. The variations of the FET parameters with bias can be understood by considering charge

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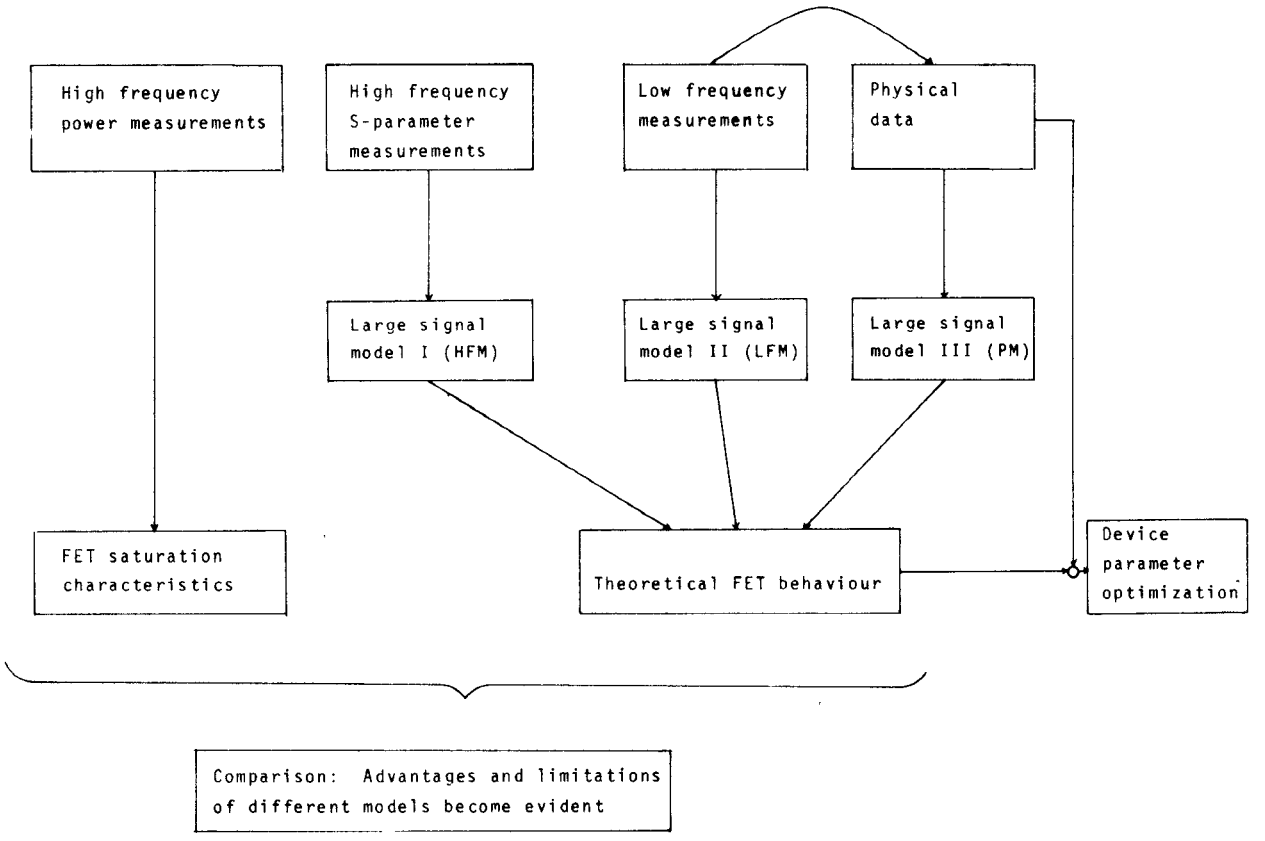


Fig. 1. Main operations for FET power optimization.

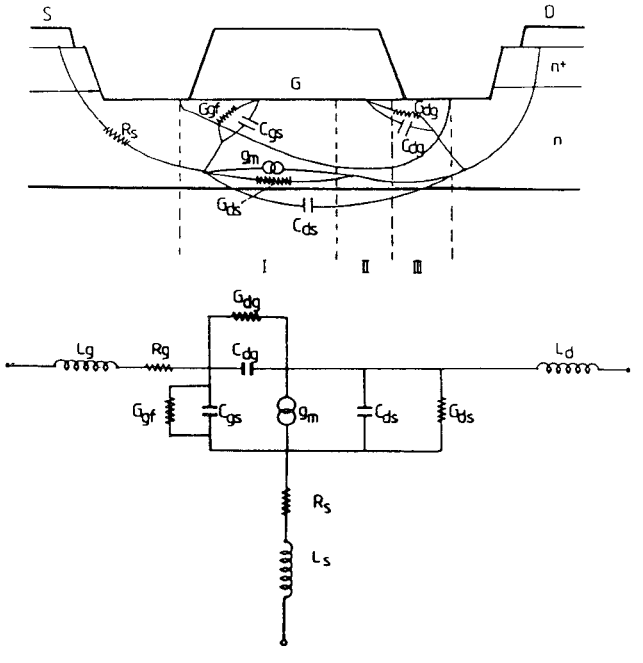


Fig. 2. FET cross section and equivalent circuit used for large-signal modeling.

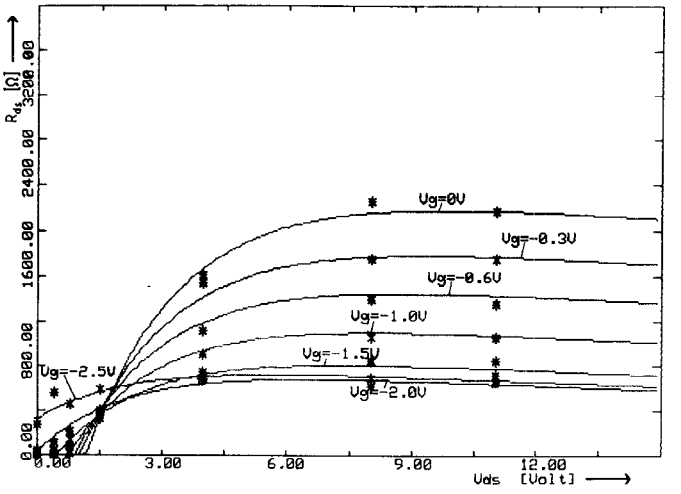


Fig. 3. Bias dependence of output resistance $R_{ds}=1/G_{ds}$ for the FET described in column A of Table I. * equivalent circuit values obtained by S-parameter fitting. —— calculated with mathematical expression of Appendix I.

accumulation and related effects in the device channel [2]. To evaluate the large-signal characteristics of the FET's, we first decompose the drain–source voltage V_{ds} into dc and small-signal ac components

$$V_{ds}=V_{dso}+v_{ds}\cdot\cos(\omega t+\phi_1)+v'_{ds}\cdot\cos(2\omega t+\phi'_1)+\cdots. \quad (1)$$

By doing the same for the gate–source voltage V_{gs}, we obtain

$$V_{gs}=V_{gso}+v_{gs}\cdot\cos(\omega t+\phi_2)+v'_{gs}\cdot\cos(2\omega t+\phi'_2)+\cdots. \quad (2)$$

We restricted our analysis to the fundamental frequency and neglected higher order components so that we can represent the FET by an equivalent lumped-element circuit. Its large-signal parameters C_{gs}, R_{ds}, g_m, G_{gf}, and G_{dg}

can be denoted by a vector X which is a function of input power P_{in}, output load Z_o, and bias voltages. All other elements of the equivalent circuit are considered to be constant with P_{in}. The calculation method is then as follows.

1) Assign initial values to the vector X.

2) Evaluate voltage amplitudes and phases $v_{ds}, \phi_1, v_{gs}, \phi_2$ by network analysis.

3) Calculate V_{ds}, V_{gs} by (1) and (2).

4) For the derived V_{ds}, V_{gs}, the vector component C_{gs}, g_m, and $R_{ds} = 1/G_{ds}$ can be calculated by the following equations (see Appendix II):

$$C = \int_0^{2\pi} \left[\int_0^{\omega t'} \left[-C'(V_{ds}, V_{gs}) \sin(\omega t' + \phi) \right] d(\omega t') \right] \cdot \cos(\omega t + \phi)\, d(\omega t)/\pi \quad (3)$$

$$G = \int_0^{2\pi} \left[G'(V_{ds}, V_{gs}) \cos(\omega t + \phi) \right] d(\omega t)/\pi \quad (\phi\text{: phase of voltage at element } C \text{ or } G). \quad (4)$$

$G' = G'(V_{ds}(\omega t), V_{gs}(\omega t))$, $C' = C'(V_{ds}(\omega t), V_{gs}(\omega t))$ give the time-dependent small-signal elements and have been obtained by curve fitting. For example, the small-signal FET output resistance R_{ds}, measured in the 2–18-GHz range, is plotted as a function of the bias voltages V_{dso}, V_{gso} together with the corresponding fitted curves in Fig. 3. This was achieved by minimizing the quadratic differences between measurements and fitting function values at 49 bias points. Results were also valid slightly outside the measurement range. The same can be done for small-signal parameters g_m and C_{gs}.

The remaining vector components G_{dg} and G_{gf} are calculated by functions based on dc measurements, as described in Section III.

The derived values $f(X)$ of the vector X can now be used as new starting values at step 1 of our procedure. This iteration continues until amplitudes and phases remain constant.

The iterative method described above is not very efficient at large input power levels, where the nonlinearities of the elements are pronounced. At input powers exceeding a certain level, it is therefore better to solve a vector equation $f(X) - X = 0$ by minimizing $(f(X) - X)^2$ to zero.

One can now predict the dependence on the input power P_{in} of the FET large-signal parameters $X_{LS} \cdot (P_{in}, f, Z_o, V_{dso}, V_{gso})$ at different frequencies f and various load terminations Z_o, and it is possible to determine gain and output power saturation characteristics. The method presented here relies entirely on high-frequency S-parameter measurements of FET's for different bias conditions, with the exception of the gate diode conductance G_{gf} and gate drain conductance G_{dg}; these are evaluated by dc measurements, as shown in the next section. Typical large-signal characteristics predicted by the above method are given in Section V.

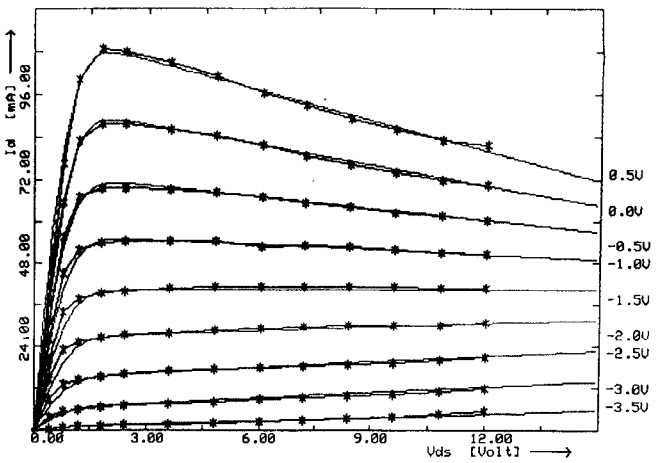


Fig. 4. I–V characteristics of FET described in column B of Table I. * measurements. —— fitting (7).

III. Determination of FET Large-Signal Parameters by DC Measurements: Low-Frequency Model (LFM)

Tajima *et al.* [3], [4] proposed a large-signal GaAs FET model based on analytical expressions of nonlinear elements derived by dc characterization. The large-signal g_m and G_{ds} parameters can be calculated from measured $I_{ds}(V_{ds}, V_{gs})$ curves (see [3])

$$g_{m-ex} = \int_0^{2\pi} \left[I_{ds}(t) \sin(\omega t + \phi_1) \right] d(\omega t) \Big/ \left[\pi v_{gs} \cdot \sin(\phi_1 - \phi_2) \right] \quad (5)$$

$$g_m = g_{m-ex}/(1 - g_{m-ex} R_s)$$

(g_{m-ex}: extrinsic value, g_m: intrinsic value)

$$I_{ds}(t) = I_{ds}(V_{ds}(t), V_{gs}(t))$$

$$G_{ds} = \int_0^{2\pi} \left[I_{ds}(t) \sin(\omega t + \phi_2) \right] d(\omega t) \Big/ \left[\pi \cdot v_{ds} \cdot \sin(\phi_2 - \phi_1) \right] \quad (6)$$

where I_{ds} is given in the form of an analytical expression derived by curve fitting measured I–V characteristics. The following function was found to best simulate the investigated implanted FET's:

$$k = 1 - (1 - \exp[-m])/m, \quad V_p = V_{po} + q \cdot V_{ds}$$

$$V_{gsn} = (1 + V_{gs}/V_p), \quad V_{dsn} = V_{ds}/V_{dssk}$$

$$G_d = g_{do} + d \cdot V_{ds} + e \cdot V_{gs}^2$$

$$f_1 = 1 - \exp\left[-|r \cdot V_{dsn} + s \cdot V_{dsn}^2 + t \cdot V_{dsn}^3| \right]$$

$$f_2 = 1/k \cdot \left(1/m \cdot \left(V_{gsn} - \left(1 - \exp\left[-m \cdot V_{gsn} \right] \right) \right) \right)$$

$$I_{ds} = I_{dsm} \cdot f_1 \cdot f_2 + G_d \cdot V_{ds} - G_d \cdot g \quad (7)$$

where r, s, t, d, e, g, k, m, q, V_{po}, V_{dssk}, and g_{do} are fitting variables; V_{po} is the value near pinch off; V_{dssk} is the value near knee voltage; and g_{do} is the value near saturated channel resistance.

An example of measured and fitted dc FET curves is shown in Fig. 4. The large-signal conductance G_{gf} can

similarly be derived through curve fitting of the experimental diode forward characteristics I_{gs} versus V_{gs}. The resulting equation is:

$$G_{gf} = \int_0^{2\pi} \left[I_{gs}(\omega t) \cdot \cos(\omega t + \phi_1) \right] d(\omega t)/(\pi \cdot v_{gs}) \quad (8)$$

where

$$I_{gs} = \begin{cases} 0, & \text{for } V_{gs} < v_1 \\ c \cdot \left(\exp\left[a \cdot (V_{gs} - b) \right] - 1, \right. & \text{for } v_1 < V_{gs} < v_2 \\ p \cdot V_{gs} + q, & \text{for } v_2 < V_{gs} \end{cases} \quad (9)$$

$$p = c \cdot a \cdot \exp\left[a \cdot (v_2 - b) \right]$$

$$q = c \cdot \left(\exp\left[a \cdot (v_2 - b) \right] - 1 \right) - v_2 \cdot p.$$

Here, a, b, and c are fitting variables.

The large-signal G_{dg} can be evaluated analogously by replacing I_{gs} in (8) by the following V_{gs}- and V_{ds}-dependent expressions fitted to measured gate–drain current characteristics:

$$R = b + c \cdot V_{gs} + d \cdot V_{gs}^2 \quad S = e + f \cdot V_{gs}$$

$$T = g + h \cdot V_{gs} \quad U = 10 \cdot k + r \cdot V_{gs} + s/10 \cdot V_{gs}^2$$

$$I_{gd} = T + S \cdot \exp\left[U \cdot V_{ds} - R \right] \quad (10)$$

where b, c, d, e, f, g, h, k, r, and s are fitting variables. Gate-to-source 1-MHz capacitance–voltage measurements can be used to obtain the following function by fitting:

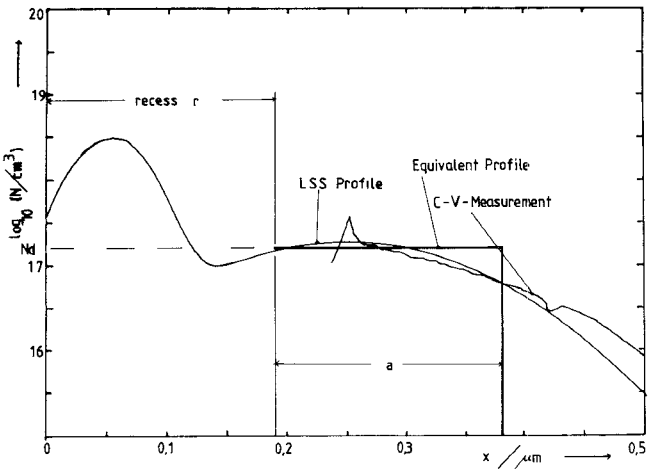


Fig. 5. GaAs FET implanted profiles ($E = 280$ keV, $D = 0.4 \cdot 10^{13}/\text{cm}^2$) calculated with LSS theory and measured with CV method together with equivalent profile used for modeling our FET's. Recess: 0.19 μm.

IV. FET Modeling for Determining Large-Signal Characteristics from Device Physical Data: Physical Model (PM)

FET dc characteristics can be determined from device physical data such as doping density, active layer thickness, and transistor geometry. Several analytical models have been proposed to analyze the performance of GaAs FET's with uniform [5] and nonuniform doping profiles [6], [7], [14].

$$C_{gs} = \begin{cases} v_1 \cdot \exp\left[-100 \cdot v_3 \cdot (0.5 + 30 \cdot v_4) \right] / \sqrt{(1 - 0.5/v_2)}, & \text{for } V_{gs} > 0.5 \\ v_1 \cdot \exp\left[-100 \cdot v_3 \cdot (V_{gs} + 30 \cdot v_4) \right] / \sqrt{(1 - V_{gs}/v_2)}, & \text{for } V_{gs} < 0.5 \\ & \text{and} \\ & C_{gs} > 0.1 \cdot C_{gk}, \\ 0.1 \cdot C_{gk}, & \text{for} \\ & C_{gs} < 0.1 \cdot C_{gk} \end{cases} \quad (11)$$

where v_1, v_2, v_3, v_4, and C_{gk} are fitting variables. Equation (3) can then be used to find the large-signal characteristics for C_{gs}, although it neglects the V_{ds} dependence of C_{gs}.

In all the above cases, the fitted expressions of the FET parameters resulted in less than 10-percent error to measured data.

Equations (3), (5), (6), and (8) give average values of small-signal parameters determined from dc measurements. These parameters refer to given V_{dso}, V_{gso}, and are to be treated as described in Section II to predict large-signal characteristics. Large-signal FET characteristics obtained by the above dc device characterization are discussed in Section V. They are valid under the condition that the frequency dependence of power-dependent elements can be neglected for small signals and that small-signal C_{gs} does not depend on V_{ds}.

The cross section of the analyzed GaAs FET's is shown in Fig. 2. The gate can be recessed by any desired amount provided that the Schottky metal does not directly contact the N^+ layer, which in our transistors extends up to 1200 Å from the surface. The depletion layer can be divided in three distinct regions: a linear region (I), a saturated region (II), and a high-field-domain region (III). Channel conductance (G_o) dc measurements of FET's with gate lengths (L) varying between 1 μm and 5 μm have sometimes demonstrated a negative shift of the $1/G_o$ versus L curve from the origin. This suggests an overall extension of the depletion layer outside the metallurgical gate by 0.2–0.8 μm, and has been taken into consideration in our modeling. The extended region is reduced in good samples with small surface state densities, resulting generally in better power performance.

Devices were analyzed by considering a double N^+–N implanted profile as predicted by LSS theory

$$n(x) = N^+ \cdot \exp\left\{-(x - Rp_1)/(\sigma_1\sqrt{2})\right\} + N \cdot \exp\left\{-(x - Rp_2)/(\sigma_2\sqrt{2})\right\} - N_t \quad (12)$$

where $N, N^+ = D/(\sigma \cdot \pi \cdot \sqrt{2})$ is the doping density at the projected range R_p of the implanted Gaussian distribution, D = dose, σ = standard deviation of Si^{29} implants, and N_t = trap density. Very good agreement was found between LSS profiles and experimental profiles determined by C–V or SIMS methods (Fig. 5). The trapping density N_t can be estimated experimentally by comparing the I–V saturation curves of a chain of ohmic contacts with equal widths but different spacings. The value of N_t is found to be proportional to the saturated current reduction $\Delta(I)$ observed for larger spacings and to be inversely proportional to the change of the square root of knee voltage $\Delta\sqrt{(V_k)}$ at which current saturation starts:

$$N_t = A \cdot \left(\Delta I/\Delta\sqrt{V_k}\right)^2 \quad (13)$$

where $A = 2 \cdot q \cdot \epsilon \cdot v_s^2 \cdot w^2$ is a constant depending on the width w of the ohmic contact test pattern (q = electron charge, ϵ = dielectric constant, v_s = saturation velocity). N_t values of ion-implanted FET's range between 10^{15} and $3 \times 10^{15}/cm^3$ [8], [9].

An equivalent uniform doping density N_d and active layer thickness a could be evaluated for every FET profile by fitting its calculated I–V curve to measured I–V characteristics or by solving the system of equations (see [6])

$$\int_r^t [N(x)\,dx] = N_d \cdot a \quad (14)$$

$$V_p = q/\epsilon \cdot \int_r^t [N(x) \cdot x\,dx] = q \cdot N_d \cdot a^2/[2 \cdot \epsilon] \quad (15)$$

where r and t represent, respectively, the recessed depth and the depletion layer thickness at pinchoff V_p. The upper limit t of the integral in (14) was evaluated for a given device by using measured V_p data and iterating until $V_p = (q/\epsilon)\int_r^t N(x)x\,dx$ (eq. 15) is satisfied. The influence of recess on FET characteristics was derived using the same t value. The $I_{ds}(V_{ds}, V_{gs})$ characteristics were evaluated by solving the nonlinear system of equations of Pucel's model [5, eqs. (7b), (18) or (11a), (18)]. In order to save computation time during large-signal calculations, we used the following analytical expression with a tanh function fitted to the latter $I_{ds}(V_{ds}, V_{gs})$ curves:

$$G = g_0 - g_1 \cdot V_{gs} + g_2 \cdot V_{gs}^2$$
$$h_1 = (V_{gs} + V_t)^{2d} \qquad (1 + c)$$
$$I_{ds} = \beta \cdot h_1 \cdot \tanh(G \cdot V_{ds}) + m \cdot V_{ds} \quad (16)$$

where $g_0, g_1, g_2, d, c, m, \beta$, and V_t are constants depending on the I–V dc characteristics to be fitted. Equation (16) was determined after modification of the Curtice formula [10] to make it more appropriate for implanted GaAs FET's.

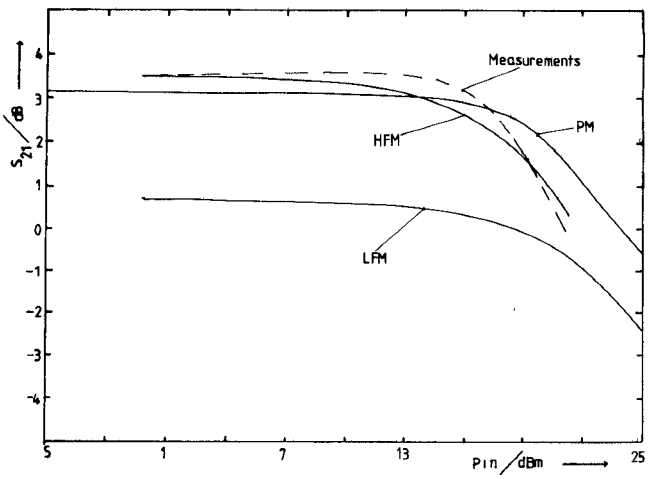


Fig. 6. Comparison of measured saturation characteristics (S_{21} versus P_{in}): physical model (PM), high-frequency model (HFM), and low-frequency model (LFM) at 10 GHz, $V_d = 4$ V, $I_d = I_{ds}/2$, and input and output impedance 50 Ω (FET: column A of Table I).

The outlined procedure permits fast calculation of large-signal characteristics with our simpified physical model. Large-signal element values are calculated as described in Section III. The drain-to-source current I_{ds} is found by using the fitted expression (16) in (5) and (6), and the gate–source capacitance C_{gs} is evaluated by the formula given in [5]. As in Section III, this procedure neglects the frequency dependencies of g_m, R_{ds} and C_{gs}. The validity of large-signal results depends also on the accuracy of the physical model used to describe the small-signal microwave behavior of the FET. All the conditions and approximations of [5] for FET modeling must also be fulfilled for our physical large-signal model. In particular, the influence of physical parameters on breakdown or avalanche characteristics, together with changes of parasitic elements is neglected.

Further, it has been assumed that the LSS profile can be replaced by a uniform equivalent profile determined by (14) and (15). A comparison of measured I–V curves with characteristics obtained by the analytical expression of (16) and the classical Pucel method [5] using (14) and (15) showed that both approaches satisfactorily approximate device properties (Fig. 6).

V. Comparison of Large-Signal FET Characteristics Obtained by Different Models

Fig. 6 shows measured and calculated gain curves of an implanted FET. The parameter values of the FET used for our physical model are listed in column A of Table I and its small-signal equivalent circuit at $V_d = 5$V and $I_d = I_{ds}/2$ is given in column A of Table II. Power saturation measurements were made at 10 GHz with the FET terminated at 50 Ω. For purposes of comparison, the transistor was modeled on the basis of high-frequency (Section II), low-frequency dc (Section III), and physical (Section IV) data.

TABLE I
PHYSICAL PARAMETERS AND FITTING VALUES FOR (16) USED TO CALCULATE THE DRAIN–SOURCE CURRENT $I_d(V_d, V_g)$ OF IMPLANTED FET's

Parameter	Value	
	A	B
W/μ	300	300
L/μ	1.5	1.5
t/μ	0.162	0.187
$N_d/(1\cdot10^{17}/cm^3)$	1.86	1.66
V_ϕ/V	0.75	0.75
$\mu_0/(m^2/V\cdot s)$	0.4	0.4
$E_s/(kV/cm)$	3.2	3.2
$\beta/(mA/V^{2d})$	3.784	5.003
d	0.670	0.715
c	3.720	1.831
m/(mA/V)	0.051	0.049
$g_0/(1/V)$	1.328	1.232
$g_1/(1/V^2)$	0.316	0.241
$g_2/(1/V^3)$	0.149	0.114
V_t/V	2.784	3.547

TABLE II
EQUIVALENT CIRCUIT ELEMENT VALUES OBTAINED FROM SMALL-SIGNAL S-PARAMETER DATA OF IMPLANTED FET's ($V_d = 5$ V, $I_d = I_{ds}/2$)

Parameter	Value	
	A	B
R_g/Ω	4.35	4.99
R_s/Ω	2.24	3.11
L_g/nH	0.090	0.035
L_s/nH	0.145	0.059
L_d/nH	0.005	0.100
C_{dg}/pF	0.041	0.021
C_{ds}/pF	0.051	0.057
C_{gs}/pF	0.415	0.324
R_{ds}/Ω	901.0	563.6
g_m/mS	29.89	24.88
τ/psec	5.43	5.16

The high-frequency modeling technique (HFM) results in large-signal FET characteristics which best fit the measured data.

The physical model (PM) predicts saturation at input power levels 5 dBm higher than the experiment. This discrepancy can be explained by its simplified form and the approximations made (Section IV). A more accurate prediction is possible by using experimental microwave data, as shown above.

The model based on low-frequency measurements (LFM) can only qualitatively describe large-signal FET behavior. One could expect it to give results at least as accurate as those of the PM, since it also uses dc data. However, the V_d dependence of the gate–source capacitance C_{gs} is neglected in the LFM (see Section II), although this is not in practice the case [5], [11]. Our low-frequency model uses an empirical formula fitted to measured data (eq. (11)) rather than the simplified theoretical formula of [3].

Similar modeling differences are observed in the characteristics of the power-dependent large-signal circuit elements. Fig. 7 shows the G_{ds}, g_m, C_{gs}, and G_{gf} variations with input power.

The dc and HF models give approximately the same small-signal g_m, while the physical model results in slightly larger values. C_{gs} and R_{ds} calculated with the PM are also larger than values obtained from the HFM. The reason for the differences of element values found with the three models is that different small-signal elements are used for the evaluation of large-signal parameters. For instance, the small-signal G_{ds} values calculated by S-parameter modeling and used in the HFM are in general larger than those obtained from I–V measurements or theoretical I–V curves (see previous sections: LFM or PM case).

In all models, g_m decreases with input power, since above a certain level the depleted region is strongly modulated near pinchoff, where g_m is relatively small. The HFM predicts g_m reductions at input power levels somewhat lower than the corresponding input power levels calculated by the other models. This is, however, believed to be realistic, since saturation also starts at lower input powers.

G_{ds} increases in general with input power, due to partial operation in the linear region of FET characteristics, where G_{ds} is large. Only the LFM shows decreasing G_d because of the measured I–V curve having a negative slope for some bias voltages (Fig. 4). The g_m and G_{ds} variations of Fig. 7(a) and (b) agree qualitatively with the results presented by Rauscher [25] and Tajima [3].

C_{gs} and G_{gf} are both predicted to increase with input power, indicating partial operation with near-zero or even positive instantaneous values of V_g. G_{dg} was always evaluated to be zero for given bias conditions.

VI. INFLUENCE OF FREQUENCY AND LARGE-SIGNAL PARAMETER INTERPRETATION

The power characteristics of ion-implanted FET's depend on the operation frequency, as illustrated in Fig. 8, where a 300-μm device is measured at 6 GHz and 12 GHz. Although the output power is practically independent of frequency (about 200 mW), the gain at the 1-dB compression point reduces from 8 dB to 4 dB with increasing frequency, following the $1/f^2$ law for G_{max}, while saturation occurs at larger input levels (+4 dBm). The power-added efficiency of the above devices was of the order of 30 percent. Since power FET's are normally operated at 5–6-dB gain, the devices of Fig. 8 will best suit a 10-GHz design where driving into saturation does not exceed 1 dB for 5–6-dB gain and power-added efficiency is consequently high.

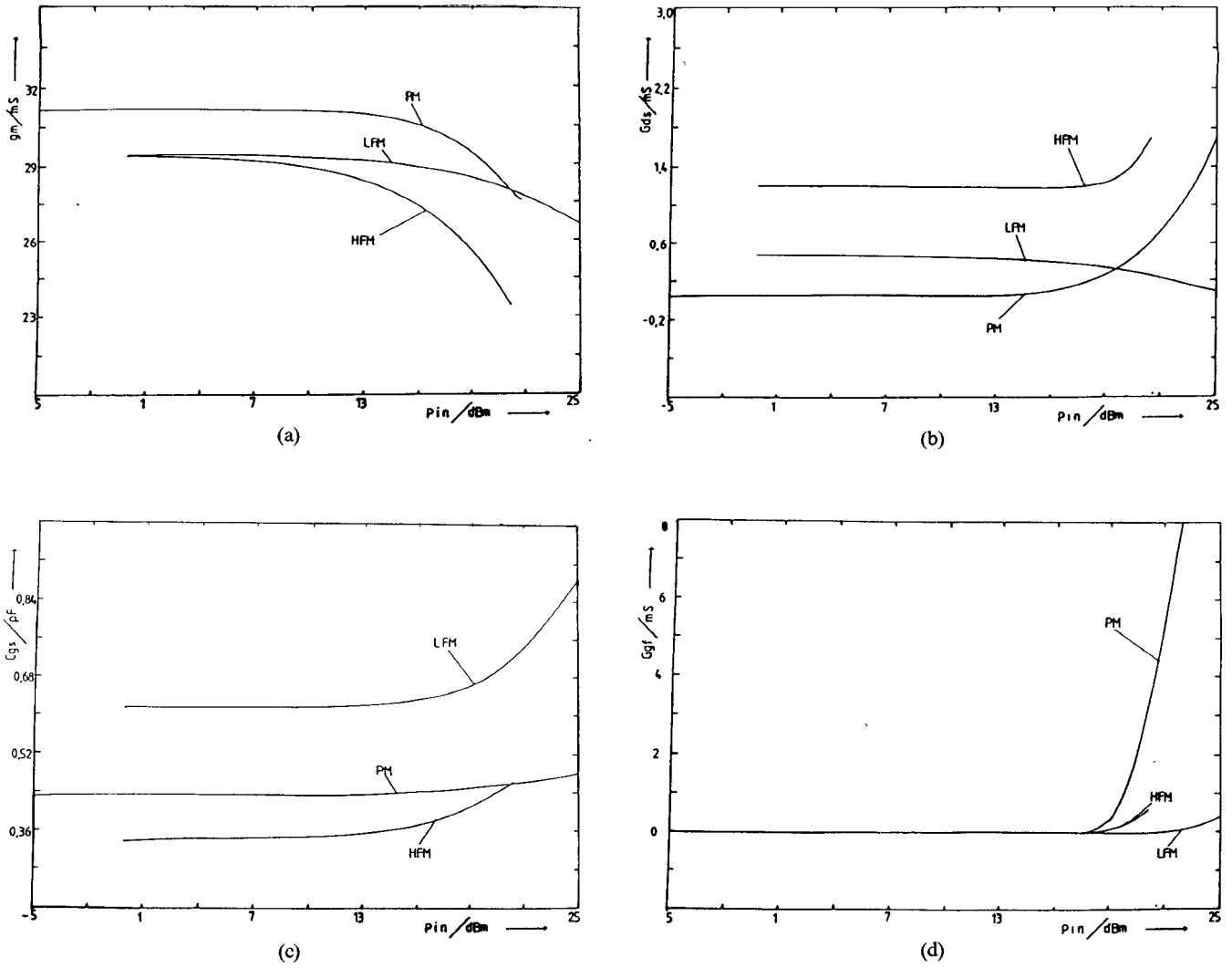


Fig. 7. Dependence of (a) transconductance g_m, (b) output conductance G_{ds}, (c) gate–source capacitance C_{gs}, and (d) gate forward conductance G_{gf} on input power predicted by the physical model (PM), low-frequency model (LFM), and high-frequency model (HFM). Modeling was made with a Table I-A FET at $f = 10$ GHz, $V_d = 4$ V, and $I_d = I_{ds}/2$.

Similar characteristics have been obtained by PM and HFM device simulation. The gain shown in Fig. 9 corresponds to a 50-Ω terminated FET ($G = S_{21}$) and therefore decreases with frequency at a different rate than $G_{\max}$. The 1-dB gain compression input power increase from 13 dBm at 2 GHz to 16 dBm at 14 GHz (HFM). This is a direct consequence of the marginal reduction of the output power at higher frequencies, while at the same time the gain is substantially reduced. The $G(P_{in})$ saturation characteristics predicted by the PM are steeper at low frequencies. This implies that driving the device to compression at high frequencies necessitates the input level much more above saturation onset than at low frequencies. In the latter case, compression is achieved by only small changes of input power, and power-added efficiency does not degrade rapidly with input level.

The large-signal parameters of the device are shown in Fig. 10. As expected, the small-signal transconductance g_m is independent of frequency. Frequency-dependent characteristics of g_m, if any, are observed in the presence of important trap densities and appear at much lower frequencies (a few tens of kHz). In large-signal operation, g_m decreases with input power (Fig. 10a). This effect takes place at almost the same input levels as the increase of channel conductance G_{ds} (Fig. 10(b)), indicating partial operation below the knee voltage, where device transconductance is smaller due to smaller carrier velocities.

The gate–source capacitance C_{gs} (not shown in the figures) increases with input power level by 60 fF for a power change from 7 dBm to 13 dBm at 2 GHz. This effect is associated with an increase of the effective channel length due to operation at higher V_{ds} voltage swings and, consequently, a shift of the charge accumulation region toward the drain.

At even higher input powers (>13 dBm), the gate–source conductance starts increasing with input power indicating gate leakage and, consequently, input signal rectification. This implies that any further increase of input power will result in additional losses across G_{gf} and will provide no output power improvement. It is worthwhile to note that

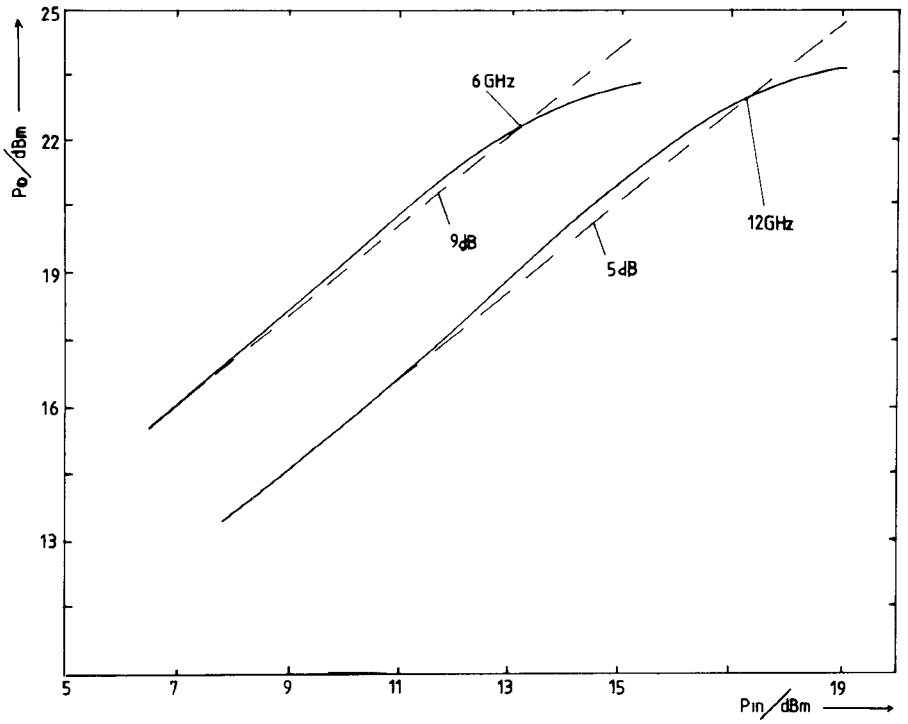


Fig. 8. Measurement of power saturation of a Table I-A FET at 6 GHz and 12 GHz ($V_d = 10$ V, $I_d = 51$ mA).

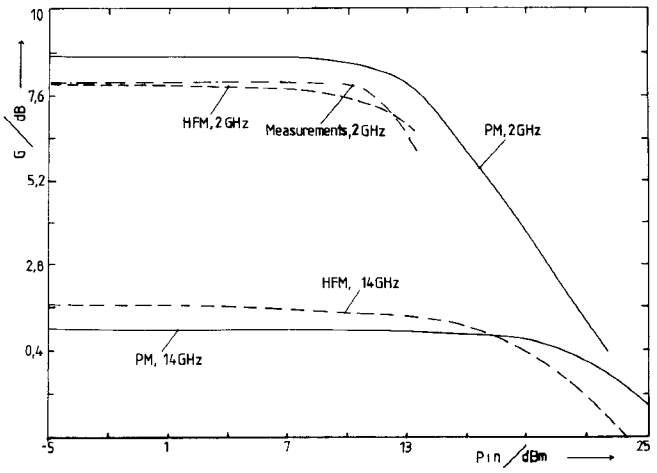
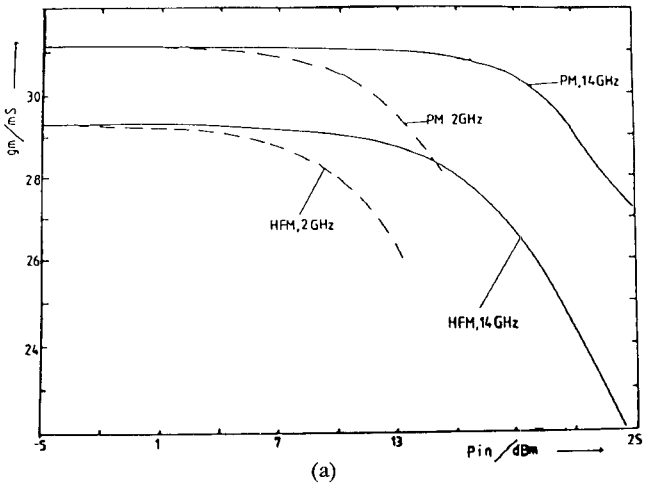
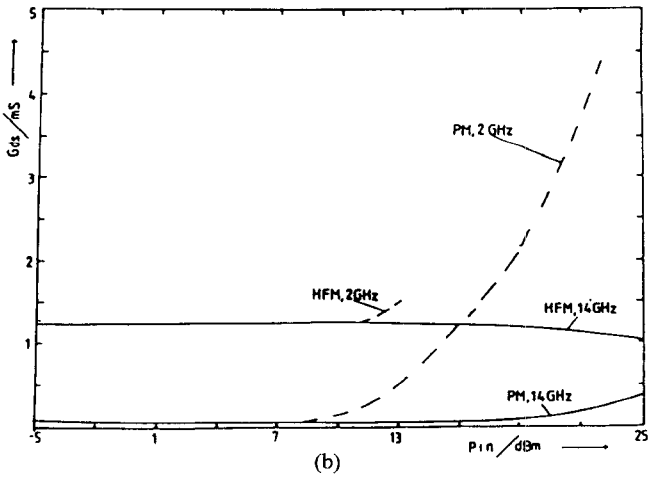


Fig. 9. Gain (S_{21})-input power characteristics of a Table I-A FET as calculated and measured at 2 GHz and calculated at 14 GHz with the HFM and PM ($V_d = 4$ V, $I_d = I_{ds}/2$, input and output impedance = 50 Ω).



(a)



(b)

Fig. 10. Dependence of (a) transconductance g_m and (b) output conductance G_{ds} on input power and frequency for a FET with saturation curves of Fig. 9.

gain saturation occurs mainly because of such gate–source losses (G_{gf}), while gate–drain breakdown effects start for the investigated transistors at a later stage. (G_{dg} was evaluated to be zero in the calculated range of operation.)

The input power level where large-signal FET parameters become power-dependent varies with the operation frequency. The higher the frequency, the wider the input power range over which the device can be used with constant large-signal characteristics. This can be understood by considering the origin of the large-signal parameter nonlinearities. Most of them result by integration of the voltage-dependent (V_{ds}, V_{gs}) small-signal device characteristics over a signal period. Higher frequency of operation will therefore require larger voltage swings in order to

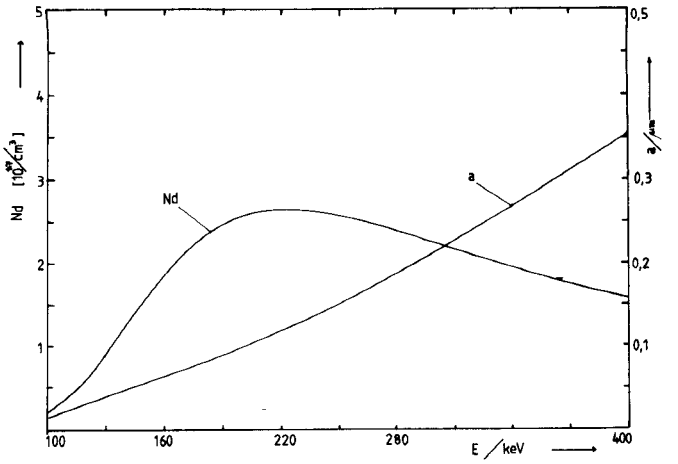


Fig. 11 Dependence of equivalent uniform doping profile N_d and active layer thickness a on implantation energy E.

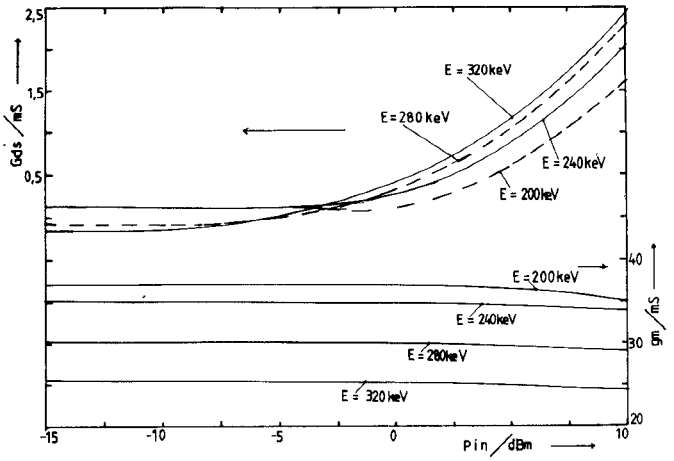


Fig. 12. Dependence of output conductance G_{ds} and transconductance g_m on input power and implantation energy at 10 GHz for a FET described in column B of Table I ($V_d = 4$ V, $I_d = I_{ds}/2$, input impedance = 50 Ω, output impedance matched for every input power).

produce the same magnitude of nonlinearity within a shorter time.

VII. Influence of Implantation Energy on Saturation

We simulated the large-signal behavior of FET's having active layers realized with different implantation energies. The projected range R_p and its standard deviation σ were determined according to LSS theory and used to solve (14) and (15) to obtain the effective active layer thickness a and the uniform doping density N_d (Fig. 11). Figs. 12 and 13 show the large-signal characteristics of g_m, G_{ds}, and gain for implantation energies between 200 keV and 320 keV. Saturation is mainly due to the G_{ds} increase with input power. C_{gs} (not shown in the figures) is more or less constant with input power. The parameter g_m decreases slightly with power for energies up to 240 keV (Fig. 12) and remains more or less constant at higher energies.

The dependence on implantation energy is very small for G_{ds}. Little variation is seen in g_m for energies close to 200 keV, decreasing more rapidly above 240 keV. C_{gs} diminishes with energy due to the increase of active layer

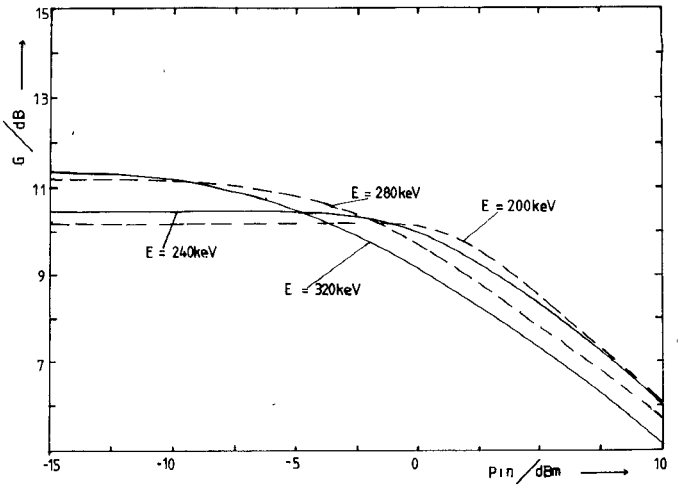


Fig. 13. Dependence of gain on input power and implantation energy at 10 GHz of a Table I-B FET ($V_d = 4$ V, $I_d = I_{ds}/2$, input impedance = 50 Ω, FET output impedance matched for maximum output power).

thickness (Fig. 11). One can consequently optimize the FET cutoff frequency $f_T = g_m/(2 \cdot \pi \cdot C_{gs})$ by choosing energies around 240 keV, where g_m is still large while C_{gs} is already sufficiently small.

As demonstrated by the results of Fig. 13, there is an optimum implantation energy to maximize the output power for a given input level. Small implantation energies are suitable only in the presence of high input powers. This is a direct consequence of G_{ds} remaining constant up to higher power levels for small energies.

VIII. Carrier Density Influence of FET Power Saturation

We present here results obtained with our physical model giving the influence of carrier density N_d on the FET large-signal characteristics. In all calculations, avalanche and current breakdown characteristics have been considered independent of doping density [17] (see Section IV). Consequently, results presented in this section underestimate the influence of doping on the FET behavior.

Fig. 14 shows the dependence of the gain on input power for different frequencies and equivalent carrier densities. Variations of the equivalent uniform doping profile N_d used for our model correspond to variations of the implanted dose D. Small-signal gain generally increases with doping density. At 10 GHz and 14 GHz, an increase of N_d from $1 \times 10^{17}/\text{cm}^3$ to $2.2 \times 10^{17}/\text{cm}^3$ gives a small-signal gain increase of about 1.0 dB. Saturation occurs earlier for higher doping densities: $P_{in} = -5$ dBm for $N_d = 2.2 \times 10^{17}/\text{cm}^3$; $P_{in} = -3$ dBm for $N_d = 1 \times 10^{17}/\text{cm}^3$. It is interesting to note that when the transistor is driven strongly into saturation, the highest doping concentration does not necessarily imply highest gain. There is in fact an optimum concentration for maximum saturated gain, as confirmed by the experimental results of Macksey *et al.* [16]. As shown by the results of Fig. 14, $N_d = 1.4 \times 10^{17}/\text{cm}^3$ is best for input powers from 2 dBm to about 5 dBm while for P_{in} smaller than 1.5 dBm, a carrier density of $1.8 \times 10^{17}/\text{cm}^3$ gives highest gain.

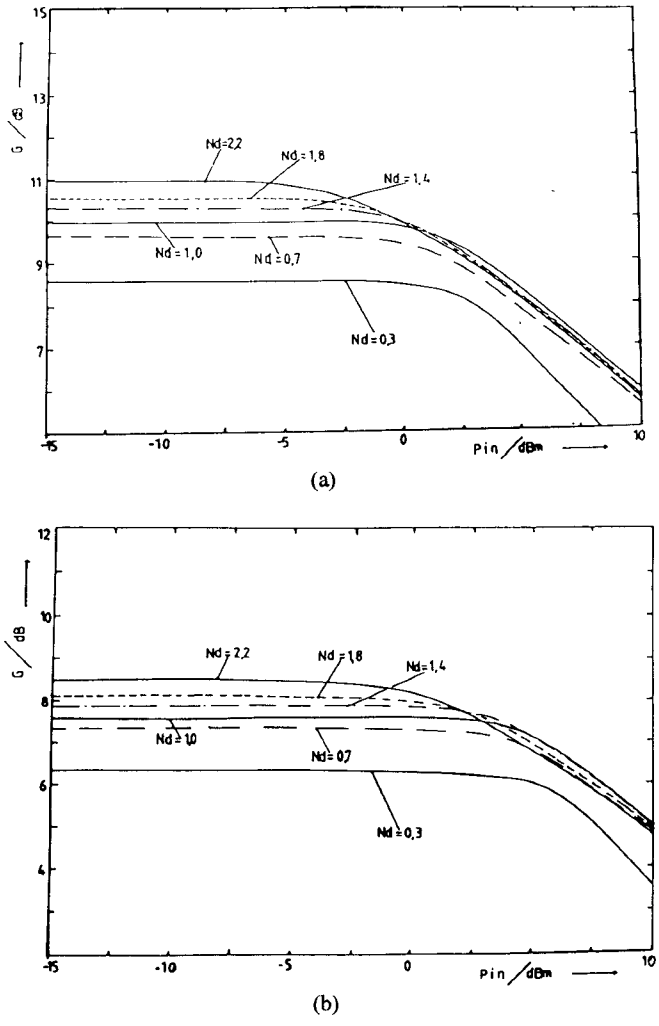


Fig. 14. Dependence of gain on input power for various equivalent doping densities of a Table I-B FET at (a) 10 GHz and (b) 14 GHz ($V_d = 4$ V, $I_d = I_{ds}/2$, input impedance = 50 Ω, output impedance matched for maximum output power).

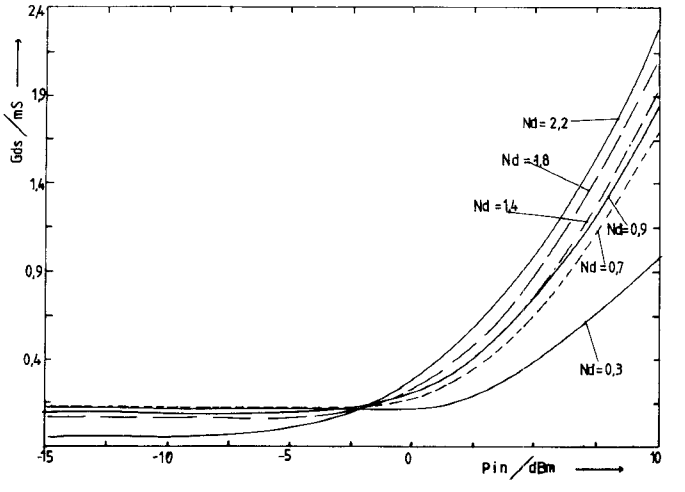


Fig. 15. Dependence of output conductance G_{ds} on input power for various equivalent doping densities of a Table I-B FET at 10 GHz ($V_d = 4$ V, $I_d = I_{ds}/2$, input impedance = 50 Ω, output impedance matched for maximum output power).

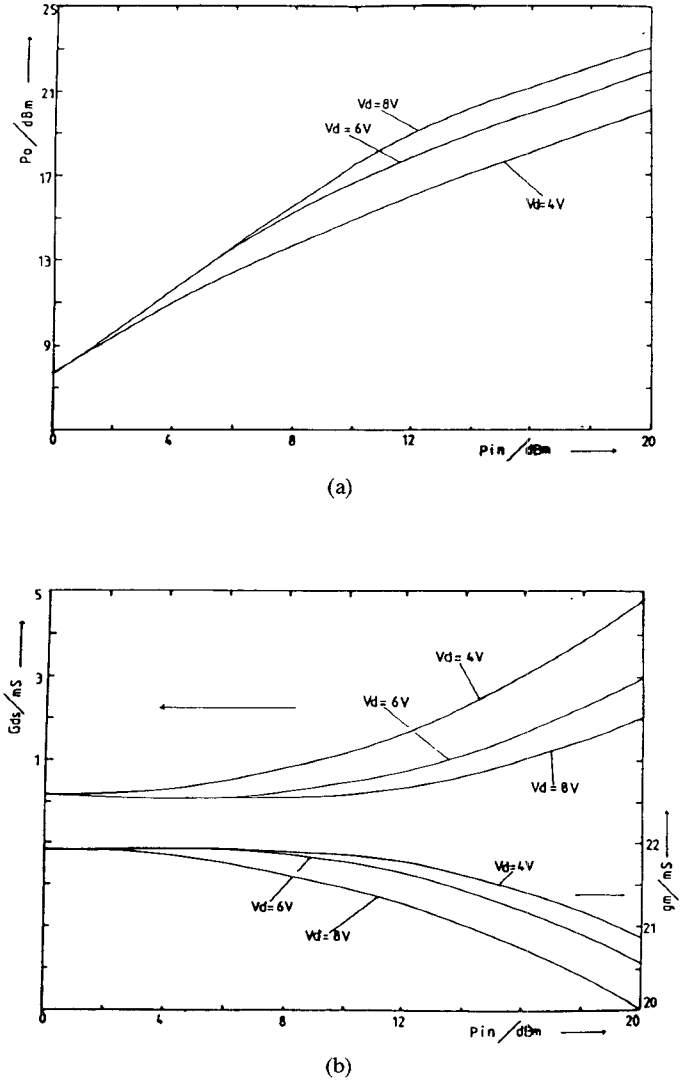


Fig. 16. (a) Output versus input power characteristics of Table I-B FET calculated at different V_d at 14 GHz ($I_d = I_{ds}/2$, input impedance = 50 Ω, output impedance matched for every input power). (b) Input power dependence of output conductance G_{ds} and transconductance g_m.

For optimum power operation at a specific gain, such as 8 dB, there is also an optimum doping. At 14 GHz, a doping of $N_d = 2.2 \times 10^{17}/\text{cm}^3$ seems preferable, while $N_d = 0.3 \times 10^{17}/\text{cm}^3$ is better for 10-GHz operation.

The earlier saturation of higher doped FET's can be understood by the large-signal characteristic of the output conductance G_{ds} (Fig. 15). At small-signal operation, G_{ds} depends only slightly on doping density. When the FET is operated at large input powers, G_{ds} increases rapidly with P_{in}. This change is particularly large for highly doped channels resulting in earlier saturation.

To estimate the influence of drain bias, saturation curves have been calculated for $V_{dso} = 4$, 6, and 8 V with $N_d = 0.9 \times 10^{17}/\text{cm}^3$ (Fig. 16(a)). Output power increases with V_{ds}, and saturation is mainly due to G_{ds} increase and g_m decrease (Fig. 16(b)). The value of the large-signal G_{dg} parameter remained zero up to $V_{dso} = 8$ V.

IX. Influence of Recess on Saturation

The influence of recess depth r can be investigated using the physical model (Section IV) and (14) and (15). Fig. 17 gives solutions for these equations for different r's. N_d can

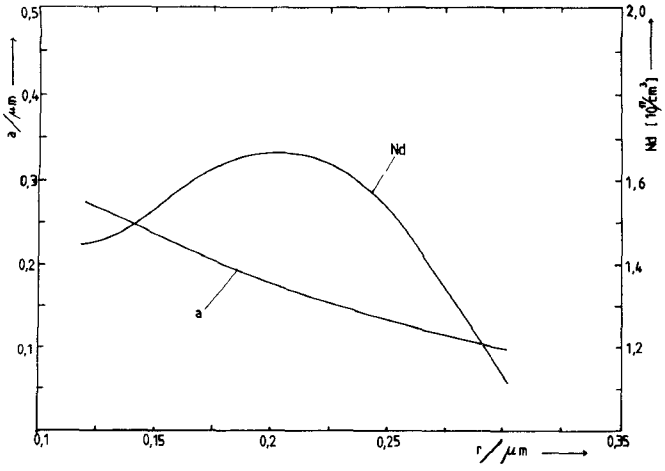
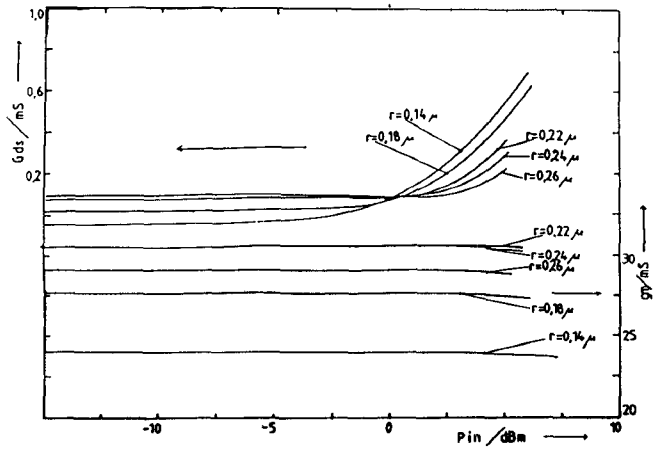
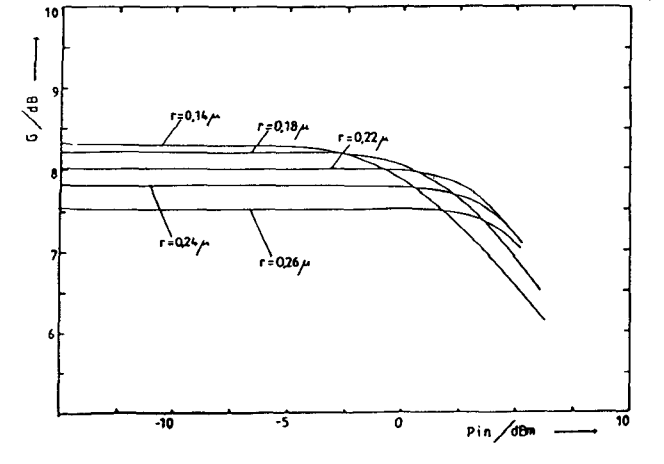


Fig. 17. Dependence of effective active layer thickness a and effective uniform doping density N_d on recess depth r.

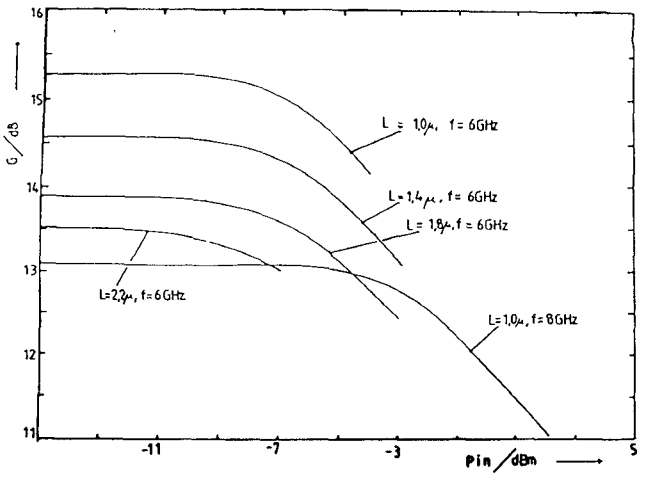


(a)

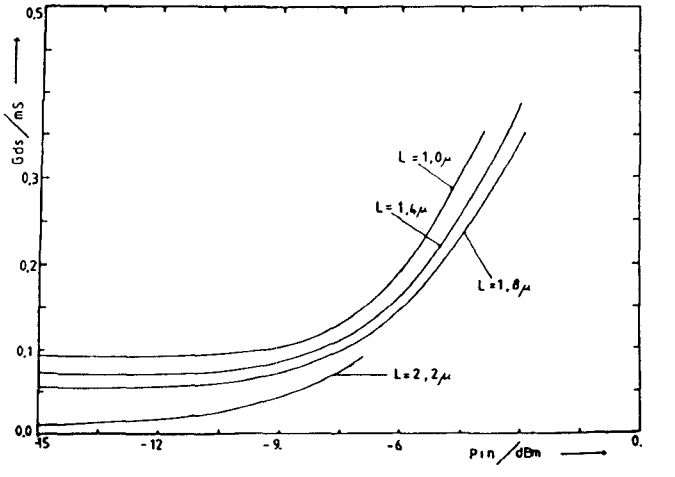


(b)

Fig. 18. (a) Output conductance G_{ds} and transconductance g_m dependence on input power for a Table I-B FET at 14 GHz ($V_d = 4$ V, $I_d = I_{ds}/2$, input impedance = 50 Ω, output impedance matched for every input power) for different recess depths r. (b) Gain dependence on input power for the same FET as a function of recess depth.



(a)



(b)

Fig. 19. Dependence of (a) gain and (b) output conductance G_{ds} on input power for different gate lengths of a Table I-B FET at 6 GHz ($V_d = 4$ V, $I_d = I_{ds}/2$, input impedance = 50 Ω, output impedance matched for maximum output power.)

be considered to be constant around R_p; consequently, the accompanying changes in FET behavior are due to changes of active layer thickness. For recesses larger than 0.22 μm, not only the active layter thickness but also the doping density diminishes.

As in the case of FET's implanted with different energies, saturation is mainly due to G_{ds} increase. C_{gs} and g_m remain constant up to the considered power levels (Fig. 18(a)).

For given implantation energies, g_m increases with recess for depths up to about 0.22 μm and then reduces slightly (Fig. 18(a)). This is confirmed by small-signal low- and high-frequency measurements. C_{gs} increases due to smaller active layer thicknesses at larger recesses.

In accordance with the results for the equivalent circuit elements, small-signal gain decreases with recess (Fig. 18(b)). Similar recess characteristics have been experimentally obtained by Tayrani [15] and Macksey *et al.* [16].

For a given frequency and input, there is an optimum recess depth for maximum output power. For input powers

from about -3 dBm to about 0.5 dBm, a recess of 0.18 μm gives highest gain, while for input levels from 0.5 dBm to about 4 dBm, $r = 0.22$ μm is best. Experimental evidence of this is given by Macksey *et al.* [16].

All parasitic elements have been considered to be constant in the recess calculations, in spite of the fact that elements such as R_s are in reality expected to diminish. FET performance (Fig. 18(b)) is therefore underestimated.

X. Gate Length Influence

The gate length influence on power saturation can be investigated with our physical model. Fig. 19(a) shows the gain saturation of transistors with different gate length. Both small- and large-signal gains increase by reducing the gate length; at 6 GHz, a reduction from $L = 2.2$ μm to $L = 1.0$ μm gives about 2 dB more gain. Qualitatively, this observation is confirmed by the large-signal-gain experimental data of Macksey *et al.* [18].

Saturation seems to be almost independent of gate length, occurring at about the same input level for all the devices. For given device gain and frequency of operation, there is an optimum gate length best suiting the desired operating conditions. For example, 1.0-μm gate length is necessary for 12-dB compressed gain at 8 GHz, while devices slightly exceeding $L = 2.2$ μm are required for the same gain at 6 GHz (Fig. 19(a)).

The dependence of equivalent circuit elements on gate length and input power can be used to explain the results of Fig. 19(a). The increase of gain with decreasing gate lengths is mainly due to smaller gate–source capacitances and larger g_m's. These parameters remain constant with input power up to gain compressions of 2 to 3 dB. Gain saturation is mainly due to an increase of G_{ds} (see Fig. 19(b)).

XI. Conclusions

Three different large-signal models using simple transistor equivalent circuits have been developed and compared with one another. All models were applied to ion-implanted MMIC-compatible GaAs FET's with regard to optimization of their power characteristics. The results obtained were confirmed by experiments.

The HFM relies entirely on small-signal S-parameter measurements obtained with different V_{gso}, V_{dso} bias conditions. The PM uses device physical data. Its results compare less satisfactorily with measured data than in the HFM case, but device characterization and subsequent calculation are easier. The final model (LFM) relies on I–V and low-frequency capacitance measurements. Device characteristics can be obtained with equal ease, but modeled FET characteristics can only qualitatively reproduce experimental saturation measurement data.

The HFM and PM have been used to investigate the role of FET parameters on its power saturation characteristics. FET saturation occurs at larger input levels at higher frequencies, smaller implantation energies, smaller doping densities, and larger recess depths. By decreasing the gate length, both small- and large-signal gains increase in an analogous way. Higher drain bias results, as expected, in larger saturated output powers, provided that the drain bias is such that no drain source leakage can occur. With optimum recess, implantation energy, and doping density, a maximum power can be obtained at any desired gain and input power. Large-signal and saturation mechanisms can be understood by the changes of equivalent circuit elements with input power. For this bias conditions considered, saturation starts in all cases due to an increase of output conductance G_{ds}. Above the saturation point, the transconductance g_m begins to decrease with input power. Finally, at even larger levels, G_{gf} and C_{gs} increase with power, indicating that the gate–source diode is partially forward biased.

The large-signal modeling procedures described in this paper have been used in order to optimize GaAs implanted FET's with respect to their power and gain characteristics.

Appendix I
Mathematical Expressions to Fit Small-Signal Equivalent Circuit Elements

The fitting criterion for the parameters given below is the minimization of the quadratic differences between measurements and fitting function values.

1) Fit function for C_{gs} with 11 fitting parameters $a \cdots l$:

$$F_1 = a + b \cdot V_{ds} \qquad F_5 = F_2 - \exp(F_1 - F_3 \cdot V_{ds})$$
$$F_2 = c + d \cdot V_{ds} \qquad F_6 = i \cdot V_{gs} / (k + V_{gs})$$
$$F_3 = -e + f \cdot V_{ds} \qquad C_{gs} = F_4 \cdot F_5 + 1 \cdot V_{gs} \cdot F_6.$$
$$F_4 = g + h \cdot V_{ds}$$

2) Fit function for R_{ds} with 12 fitting parameters $a \cdots m$:

$$F_1 = a + b \cdot V_{ds} + c \cdot V_{ds}^2 \qquad F_4 = i(k - \exp(1 - V_{ds}))$$
$$F_2 = d + e \cdot V_{ds} + f \cdot V_{ds}^2 \qquad F_6 = k + m \cdot V_{ds}$$
$$F_3 = g + h \cdot V_{ds}$$
$$R_{ds} = 1000 \cdot \left(F_1 \cdot \left(1 - \exp\left(F_3 + F_6 \cdot V_{gs}\right)\right) + F_4 \cdot V_{gs} + F_2.\right.$$

3) Fit function for g_m with 11 fitting parameters $a \cdots l$:

$$F_1 = a + b \cdot V_{ds} + c \cdot V_{ds}^2 \qquad F_4 = 1 - \exp(F_3 - h \cdot V_{gs})$$
$$F_2 = d + e \cdot V_{ds} \qquad F_5 = i + k \cdot V_{ds} + 1 \cdot V_{ds}$$
$$F_3 = f + g \cdot V_{ds} \qquad g_m = F_4 \cdot F_5 + F_1 \cdot V_{gs}.$$

Appendix II
Equations Relating Small- and Large-Signal FET Parameters

The value of the total instantaneous voltage V_i across the complex impedance Z_i can be determined by the following expression after neglecting higher order terms:

$$V_i = V_{io} + v_i \cdot \cos(\omega t + \phi_i) = V_{io} + v_i'(\omega t). \qquad \text{(A1)}$$

Similarly, we can write for the instantaneous current

$$I_i = I_{io} + i_i'(\omega t). \qquad \text{(A2)}$$

The ac current through a conductance $G(\omega t)$ of the FET model is

$$i_i(\omega t) = i_i \cdot \cos(\omega t + \phi_i) = v_i \cdot G'(\omega t) \cdot \cos(\omega t + \phi_i). \quad \text{(A3)}$$

The total charge on a FET capacitor is given by

$$Q = C_{ls} \cdot v_i = \int_o^{V(\omega t_o)} C'(\omega t)\, dV$$

$$= v_i \cdot \int_o^{\omega t_o} - C'(\omega t) \cdot \sin(\omega t + \phi_i)\, d(\omega t). \quad \text{(A4)}$$

Several iterations are necessary in order to evaluate the large-signal values of the FET. For each particular iteration, large-signal conductance G_{ls} and capacitance C_{ls} can be calculated by multiplication of equations A3 and A4 with $\cos(\omega t + \phi_i)$:

$$G_{ls} = v_i / i_i = 1/\pi \cdot \int_o^{2\pi} G'(\omega t) \cdot \cos^2(\omega t + \phi_i)\, d(\omega t) \quad \text{(A5)}$$

$$C_{ls} = 1/\pi \cdot \int_o^{2\pi} \left(\int_o^{\omega t_o} - C'(\omega t) \cdot \sin(\omega t + \phi_i)\, d(\omega t) \right) \cdot \cos(\omega t_o + \phi_i)\, d(\omega t_o). \quad \text{(A6)}$$

These equations now permit the calculation of large-signal FET parameters by successive iteration.

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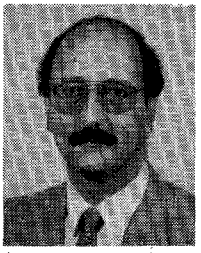

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